wave Techniques COMITE 2015, April 22-23, Pardubice, Czech Republic, pp. 183-186.

9. L'vov, A.A. Statistical Approach to Measurements with Microwave Multiport Reflectometer and Optimization of Its Construction / A.A. L'vov, R.V. Geranin, N. Semezhev, P A. L'vov // Proceedings of Microwave and Radio Electronics Week (MAREW 2015). 14th Conference on Microwave Techniques (COMITE 2015), Pardubice, Czech Republic, April, 22 - 23, 2015, P. 179-183.

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CALIBRATION ALGORITHMS FOR SOFTWARE DEFINED RADIO APPLICATIONS

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1. Introduction

Today the evolution toward practical software radios is accelerating through a combination of techniques. These include smart antennas, multi-band antennas, and wideband RF devices. Nowadays wideband analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) can access GHz of spectrum instantaneously, Intermediate Frequency (IF), base-band, and bit stream processing is implemented in increasingly general purpose programmable processors with Application-Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), Digital Signal Processors (DSPs), and general purpose (GP) processor technologies are being introduced in SDR designs. SDR is becoming practical as costs per millions of instructions per second (MIPS) of DSPs, and general-purpose central processor units (CPUs) have dropped below $10 per MIPS. The economics of software radios become increasingly compelling as demands for flexibility increase while numerical processing costs continue to drop by a factor of two every few years but RF parts and sub-assembly costs tend to remain high particularly at millimeter wave frequencies. At the same time, absolute processing capacities continue to climb into the hundreds of millions of floating-point operations per second (MFLOPS) to billions of FLOPS (GFLOPS) per chip. At present time, software radio technology can be cost-effectively implemented for commercial first-generation (1G) analog and second-generation (2G) digital mobile cellular radio air interfaces. Over time, wideband third generation (3G) air interfaces will also yield to software techniques on wideband RF platforms possibly at millimeter wave frequencies. The resulting software-defined radio extends the evolution of programmable hardware, increasing flexibility via increased programmability. The ideal software radio represents the point of maximum flexible programmability in this evolution. In addition, ADCs and DACs are available as low-cost chips and single-board open-architecture configurations offer bandwidths of tens of MHz with the dynamic range required for software radio applications. Multimedia requirements for desktop and wireless personal digital assistants (PDAs) continue to exert downward pressure on parts count and on power consumption of such

chip sets. This trend will push the ideal software radio technology from the base station to the mobile terminal. Although the tradeoffs among analog devices, low-power ASICs, DSP cores, and embedded microprocessors in handsets remain fluid, cutting-edge base stations are beginning to employ software radio architectures. New designs for high-end mobile radio nodes such as military vehicular radios are now largely based on some type of software radio approach.

Finally, the multi-band, multi-mode, and multi-user flexibility of software radios appears central to the goal of seamless integration of personal communications systems (PCS), land mobile and satellite mobile services (including truly nomadic computing). Compared to the traditional hardware radio, the main advantage of software radio is the fact that it can support various modulation schemes with a unique hardware. On the other hand, its main disadvantage is still the present high cost of digital programmable devices. This situation can change with the rapid development in semi-conductor processing technology and the development of re-configurable devices in combination with six-port receiver technology [2].

2. Calibration

It is possible to calculate the ratio of amplitude, frequency and phase between LO signal (port 1) and RF signal (port 2) from the four output power levels determining the complex constants X_i, Y_i by calibration procedures. We now examine the six-port calibration method and the six-port receiver demodulation results obtained with calibration. Among the many algorithms that have been proposed for the physical calibration of six-port reflectometers (SPR's) [7], Engen's six-port-to-four-port reduction [5], [1] seems to be the most attractive. This procedure determines the dependencies between the different power meter readings, yielding five real-valued reduction parameters that permit to transform the SPR into a virtual four-port. No known standards are required for this reduction. The value measured by the virtual four-port is related to the reflection coefficient of the device under test by a so-called "error box" transformation. The three complex parameters of this transformation may be found by using one of the many existing methods for the calibration of traditional network analyzers. Recently, some real-time six-port calibration algorithms were proposed. These calibration algorithms are designed for six-port direct receivers, a brief description of these calibration methods are given here.

3. Physical six-port calibration method

W-plane calibration of six-port circuit

Using the same annotation as Stumper [3], the six-port to four-port reduction is given by the equations

$$p_1 = |w|^2 \quad (1)$$

$$Zp_2 = |w - w_1|^2 \quad (2)$$

$$Rp_3 = |w - w_2|^2 \quad (3)$$

where w is the complex reflection coefficient at the input of the imaginary ideal four-port reflectometer and the p_i denote the power levels p_1 to p_3, measured with the SPR significantly.

However, good initial estimates of the five parameters are needed for measured at the ports labeled 1 to 3, normalized with respect to the power value measured at the reference port 4 of the SPR. The five reduction parameters to be determined by the calibration are the values of the real positive variables *Z*, *R*, and w_1, and the real and imaginary parts of the complex variable w_2.

The variable may be eliminated from (1) to (3) yielding the nonlinear constraint equation

$$Ap_1^2 + BZ2p_2^2 + CR2p_3^2 + (C-A-B)ZP_1P_2 + (B-C-A)RP_1P_3 + \\ + (A-B-C)ZRP_2P_3 + A(A-B-C)P_1 + B(B-C-A)ZP_2 + \\ + C(C-A-B)RP_3 + ABC = 0 \quad (4)$$

where

$$A = |w - w_2|^2 \quad (5)$$

$$B = |w - w_2|^2 \quad (6)$$

Equation (4) can be solved by measuring at least nine (usually 13 in practice) arbitrary different terminations. The solution of (4) [*A, B, C, Z, R*] allows transformation of six-port to a perfect four-port reflectometer in a notional "W" complex plane. The W-plane reflection coefficient is

$$W = \frac{p_1 - Z^2 p_2 + C}{2\sqrt{C}} + j\frac{[C(A+B-C)+(A-B+C)p_1 - (A-B-C)Z^2 p_2 - 2CR^2 p_3]}{\pm 2\sqrt{C(2AB+2BC+2AC-A^2-B^2-C^2)}} \quad (7)$$

Error-box calibration

A two-port error box is inserted between the notional four-port and the DUT such that the virtual reflection reading from the notional perfect reflectometer obtained by W-plane calibration are transferred to the real reflection coefficients Γ[6]. This is done through a bilinear transformation

$$\Gamma = \frac{e - W}{cW - d} \quad (8)$$

where *c*, *d*, and *e* are complex constants related to the S parameters of the error box

$$c = -S_{22}$$
$$d = S_{12}S_{21} - S_{11}S_{22}$$
$$e = S_{11},$$

where S_{11}, S_{12}, S_{21}, and S_{22} are S-parameters of six port junction.

W-plane to Γ-plane bilinear transformation is shown in Fig. 1.

After six-port-to-four-port reduction and error box calibration, $|b_2|$ and Γ can be determined.

Therefore the phase difference and amplitude ratio of a_1 and a_2 can be obtained.

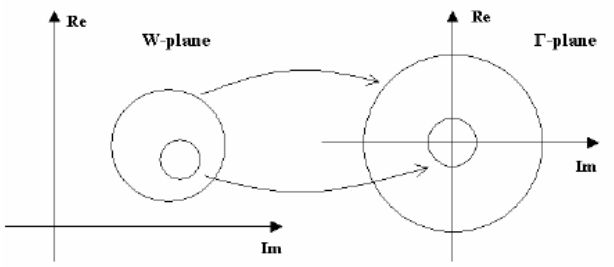


Fig. 1 W-plane to Γ-plane bilinear transformation

4. Real-time calibration method for six-port receiver[4]

Physical six-port calibration method use external physical standard terminals to its input port. However, for a six-port receiver, it would be entirely impractical. It is therefore necessary to develop a calibration method free from any external connection.

To accomplish this goal, new six-port calibration methods is achieved by feeding a RF signal other than the reference source into DUT port of the six-port. This signal can be either an unmodulated signal carrier with a frequency adjacent to the six-port local source frequency, or a digital modulated signal with a frequency equal to or close to the local source frequency. The resulting output waveforms of the diode detectors of the six-port are actually beat-signals of the two RF signals. The voltage readings corresponding to a group of widely distributed terminations are acquired by properly sampling these waveforms.

As we know, the leakage of the received signal to the local oscillator reference port is small, and may be neglected. In this case, the relationship between the output data of SPR and the three power ratios of the detectors of the six-port become linear, and can be expressed as follows:

$$\Gamma_r = A_{r1}p_1 + A_{r2}p_2 + A_{r3}p_3 + C_r \quad (9)$$

$$\Gamma_i = A_{i1}p_1 + A_{i2}p_2 + A_{i3}p_3 + C_i \quad (10)$$

where Γ_r , Γ_i are the calculated output data, whereas A_{rj} , A_{ij} (j=1,2,3) and C_r, C_i are calibration parameters to be determined. Power ratios at the output detectors of the six-port are p_1, p_2, p_3.

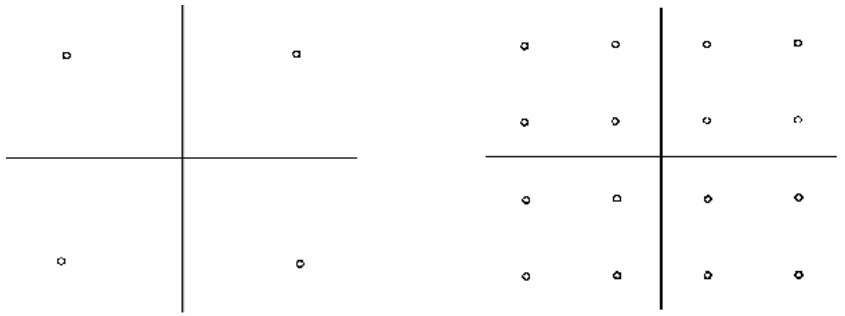
It is clear that from the above equations that a total of eight parameters should be determined from the calibration procedure. Therefore, four known sets of I, Q values or signal standards SS should be used to obtain eight linear equations for solution of the above eight parameters of calibration A_{rj} , A_{ij} and C_r, C_i. These four known sets of I, Q values are ideally selected as being the four different states in QPSK. However, simulation shows that the calculation diverges when the four known sets of I, Q values have the same amplitude. Hence, at least the amplitude of one signal standard should be different from the remaining three. Therefore, we choose three sets of I, Q values from the four states of a QPSK signal and a zero signal at the input of the re-

ceiver as the fourth known I, Q set. The zero signal input can be achieved by applying a large bias to drive the low-noise amplifier (LNA) in the receiver front end far beyond cutoff. An alternative method is to insert an attenuation for example, 3 or 6 dB in the fourth set of QPSK signal.

From the above four sets of *I, Q* values or signal standards, we have four sets of detector output power ratios of the six-port, namely, *Q* with k=1, 2, 3, 4 and j=1, 2, 3. Substituting $Q_{k,j}$ into Equation (7) and equating the left-hand *k, j* side of these equations to the standard *I, Q* values, (1, 1), (-1, 1), (-1, -1), and (0, 0) we have two systems of four linear equations. One of them corresponds to Equation (8), and the other to Equation (9). Solving these systems of linear equations, we obtain the following parameters, A_{rj} , A_{ij} j=(1, 2, 3) and C_r, C_i from which the calculations of the receiver output *I, Q* data are made using the ratios of the output readings of the power detectors in Equation (7).

5. Demodulation algorithms results

The complex constants related to six-port circuit X_i, Y_i that are obtained from calibration to arrive at required receiver demodulation. Table 1 and 2 show the simulated demodulation results for virtual six-port circuit for QPSK and QAM16 modulations when using suitable algorithms.



(a) QPSK (b) QAM16

Fig.2 Input signal constellations for QPSK and QAM16 modulation

Table 1 Demodulation data result for QPSK signal

Input	Output	Input	Output
1.0000·exp(j45°)	1.0205·exp(j46.66°)	1.0000·exp(j225°)	1.0000·exp(j224.68°)
1·exp(j 135°)	0.9595·exp(j 139.42°)	1·exp(j 315°)	1.0365·exp(j 315.45°)

Table 2 Demodulation data result for QAM16 signal

Input	Output	Input	Output
4.2426·exp(j 45°)	4.1636·exp(j 47.46°)	1.4142 exp(j 225°)	1.5123 exp(j 227.20°)
3.1623·exp(j 18.43°	3.1548·exp(j 18.90°)	3.1623 exp(j 251.56°)	3.1305 exp(j 249.71°)
1.4142·exp(j 45°)	1.2892·exp(j 43.18°)	4.2426 exp(j 225°)	4.2693 exp(j 224.02°)
3.1623·exp(j 71.56°)	2.9562·exp(j 43.15°)	3.1623 exp(j 198.43°)	3.1952 exp(j 201.29°)
3.1623·exp(j 341.57°	3.2395·exp(j 341.25°)	3.1623 exp(j 108.44°)	2.9198 exp(j 111.52°)
4.2426·exp(j 315°	4.3099·exp(j 341.82°)	1.4142 exp(j 145°)	1.2758 exp(j 143.24°)
3.1623·exp(j 288.44°	3.1222·exp(j 287.17°)	3.1426 exp(j 161.57°)	3.0527 exp(j 166.60°)
1.4142·exp(j 315°	1.4511·exp(j 311.64°)	4.2426 exp(j 145°)	3.9331 exp(j 141.67°)

The simulated demodulation results show that the receiver has an accuracy of ±5 degrees in phase and ±0.4 dB in amplitude. It is found that actual six-port circuits do indeed comply with above resolution in phase and amplitude.

6. Conclusion

The development of SDR technology based on six-port receiver scheme has been investigated and some simulations and experimental results obtained particularly at millimeter-wave frequencies are presented. The six-port based receiver can support multi-modulation and multi-band communication and it should achieve better performances than existing super-heterodyne or direct conversion receiver when coding, carrier recovery and higher level of circuit integration technology are implemented. The six-port receiver scheme is strongly motivated by the fact that the speed and present state-of-the-art re-configurable devices such as digital signal processors (DSP) and field programmable gate arrays (FPGA) are already satisfactory and increased performances with price reduction are foreseen. On the other hand, the cost of the microwave components for six-port receiver can be reduced mainly due to increased circuit integration means and six-port receiver approach. Therefore, a receiver configuration that shifts the complexity to digital signal processing and alleviates problems associated with RF components can be viable in terms of cost, functionality and market penetration.

References

1. A.A. L’vov and A.A. Morzhakov, “Statistical estimation of the complex reflection coefficient of microwave loads using a multi-port reflectometer,” Proceed. of 1995 SBMO/IEEE MTT-S International Microwave and Optoelectronic Conference, Rio-de-Janeiro, Brazil, July, 1995, vol. 2. P. 685 - 689.

2. F.M. Ghannouchi, A. Mohammadi, *The six-port technique with microwave and wireless applications*, Boston, London: Artech House, 2009.

3. J.F. Gagné, J. Gauthier, and R.G.Bosisio, “High Speed Low Cost Architecture of Direct Conversion Digital Receiver”, IEEE IMS Symposium, Phoenix, AZ, Conf. Proceedings, vol.2, pp.1093-1096, May 20-25, 2001.

4. N. Semezhev, A.A. L’vov, P.A. L’vov, et.al, "A Novel Parameter Estimation Technique for Software Defined Radio System Based on Broadband

Multi-port Receiver," Proceedings of the XI Internat. Conf. SIBCON-2015, Omsk, 2015.

5. B.M. Katz, A.A. L'vov, V.P. Meschanov, *et.al* "Synthesis of a Wideband Multiprobe Reflectometer," IEEE Transactions on Microwave Theory and Techniques, Vol. 56, No. 2, February, 2008, P. 507-514.

6. A.A. L'vov and K.V. Semenov "A Statistical Calibration Technique of the Automated Multiprobe Transmission Line Reflectometer" – Proc. 10th Intern. Conf. "Systems for Automation of Engineering and Research", 1996, St. Konstantin, Bulgaria, pp. 38-42.

7. L'vov, A.A. Statistical Approach to Measurements with Microwave Multiport Reflectometer and Optimization of Its Construction / A.A. L'vov, R.V. Geranin, N. Semezhev, P A. L'vov // Proceedings of Microwave and Radio Electronics Week (MAREW 2015). 14th Conference on Microwave Techniques (COMITE 2015), Pardubice, Czech Republic, April, 22 - 23, 2015, P. 179-183.

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DIODE POWER DETECTORS IN SOFTWARE DEFINED RADIO APPLICATIONS

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Abstract: In this paper an observation of diode power detectors in software defined radio systems is provided. The mathematical model of such detectors is discussed and its advantages are revealed. The results of computer simulation confirming the theoretical result are given.

Keywords: diode power detector, software defined radio, digital signal processing, continuous wave, modulation.

1. Introduction

In a multi-port receiver, the extremely large bandwidth and the very high maximum frequency is achieved by using semiconductor diodes in a power detector configuration. Cut-off frequencies of Schottky diodes can reach terahertz frequencies [1]. In fact, the diode based power detector can be regarded as a diode mixer with an LPF at the output. Fig. 1(a) shows the process of conventional multiplicative mixing where transistors are used for frequency conversion (i.e. in a Gilbert cell) with subsequent low pass filtering.

(a) Multiplicative mixing (b) Additive mixing (multi-port down conversion)

Fig. 1: Multiplicative versus additive mixing. The additive mixing process is the basis of the multi-port theory

The new concept that is used in multi-port receivers is based on additive mixing as shown in Fig. 1(b). In a multi-port receiver, each of the four output ports is connected to a power detector. The signal addition itself takes place in the interferometer circuit which superposes the radio frequency (RF) and local oscillator (LO) signals under different phase angles Φ_i. It is possible to make such interferometers very broadband [3]. In comparison to conventional IQ mixers with two output ports, the signals at the output ports of the power detectors must be processed further. The baseband IQ signals are calculated from the four power readings after a calibration process.

Linearization of the diode power detectors characteristics is performed to open up limitation of diode power detector's dynamic range and to extend it without affecting the received signal quality. The output voltage of the diode power detector is used to predict its characteristic and compensate for its nonlinear behavior.

2. Semiconductor Diode Circuit Model

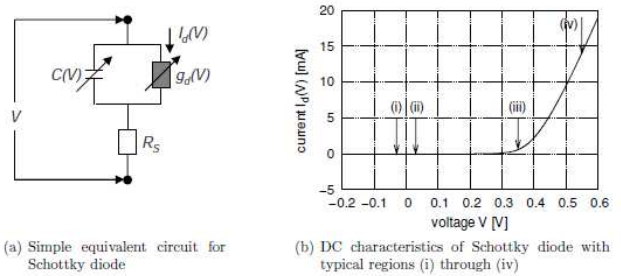
In order to understand the diode power detector, it is necessary to have a circuit model for the Schottky diode. This model has to be valid for both the large signal, nonlinear case as well as for the small signal case [2]. Since the Schottky diode is largely immune to minority carrier effects, the junction capacitance

$$C(V) = \frac{C_{j0}}{\sqrt{1 - V/\phi_{bi}}} \qquad (1)$$

and diode current

$$I_d(V) = I_s(e^{\alpha V} - 1), \qquad (2)$$

where $\alpha = e_0 V / n k_B T$, change almost instantaneously with junction voltage V (C_{j0} is the junction capacitance at zero bias); ϕ_{bi} is the built-in potential from Schottky contact; I_s is the reverse saturation current; e_0 is the charge of an electron, n is the diode ideality factor; k_B is the Boltzmann constant (1.37×10^{-23} J/K); T is the absolute temperature in Kelvin. It is typically between 10^{-6} and 10^{-15} A, and at T=290 K, α=28 mV). Therefore, the DC expressions for these quantities are valid to very high frequencies in the hundreds of GHz. In the large signal diode model, it is assumed that the capacitance and current are functions of the junction voltage alone. This is valid up to at least 250 GHz [5].



(a) Simple equivalent circuit for Schottky diode (b) DC characteristics of Schottky diode with typical regions (i) through (iv)

Fig. 2: Equivalent circuit of Schottky diode and its DC characteristics