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ANALOG TO DIGITAL CONVERTER FOR GNSS SIGNALS

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The important component in the front-end path is the analog-to-digital converter. This device is responsible for the conversion of the analog signal to digital samples. The key parameters to consider for this discussion are the number of bits, the maximum sampling frequency, the analog input bandwidth, and the analog input range.

In the development of analog-to-digital converters for circuit designs there heve been four basic types: flash, successive-approximation (SAR), pipeline, and sigma-delta converters. A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, 2N – 1, doubles with each additional bit. A successive-approximation ADC uses a comparator to successively narrow a range that contains the input voltage. At each successive step, the converter compares the input voltage to the output of an internal digital to analog converter which might represent the midpoint of a selected voltage range. At each step in this process, the approximation is stored in a successive approximation register. A pipeline ADC uses two or more steps. At first, a coarse conversion is done. In a second step, the difference from the input signal is determined with a digital to analog converter. This can be considered a refinement of the successive-approximation ADC where the feedback reference signal consists of the interim conversion of a whole range of bits. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size. A sigma-delta ADC samples the desired signal by a large factor and filters the desired signal band. Generally, a smaller number of bits than required is converted using a flash ADC after the filter. A digital filter follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. Each has its strong and weak points. The optimum device for a particular system depends on the application.

For examples the ADS830 from company Texas Instruments is a pipeline, CMOS Analog-to-Digital (A/D) converter that operates from a single +5V power supply. This converter provides performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes an 8-bit quantizer, and the ADS830 employs digital error correction techniques to provide sufficient differential linearity for imaging applications.

To compare with the ADC830 we can take for examples MAX2769. It represents the most flexible, high-performance, low-power GNSS receiver on the market. The integrated ADC outputs 1 or 2 quantized bits for both I and Q channels, or up to 3 quantized bits for the I channel. The MAX2769 features an on-chip ADC to digitize the down converted GPS signal. The maximum sampling rate of the ADC is approximately 50Msps. The sampled output is provided in a 2-bit format. The ADC supports the digital outputs in three different formats: the unsigned binary, the sign and magnitude.

There are also other types of ADCs, which include conveyor and combined types, consisting of several ADCs with different architecture. However, the above architecture of the ADCs are the most significant in view of the fact that each architecture has a definite place in the general range of speed – bit.