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WATERING CONTROL AND OPTIMIZATION USING DIFFUSED CAPACITANCE-BASED SENSING

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Measuring soil water content is essential especially for agricultural water management, where the optimization of the use of water resources is crucial and strategic for the long-term competitiveness of the agricultural industry [1]. Soil moisture content measurements may rely on different technologies. For example, a microwave soil moisture sensor using microstrip transmission line (to be placed in the soil) and an electronic transceiver was presented in [2], and algorithms for measurement were presented in [3-8]. Also time-domain reflectometry (TDR) is widely used for monitoring soil moisture content [9]; however, for traditional TDR probes, soil moisture measurement depends on the placement of the TDR probe in the sample. Capacitance sensors are widely used for soil water content where this parameter is determined by measuring the capacitance between soil implanted electrodes [10]. A comprehensive review of the methods available for estimating soil moisture and its implications for water resource management can be found in [10].

The present work considers the possibility of employing diffused, flexible sensing elements for studying soil moisture variations, based on capacitance measurements. In practical applications, such a sensing element (SE) configuration would allow following the desired path along the cultivation field. These wire-like

Ongoing work is aimed at creating an implementation of the above SDR design using available FPGA boards and conducting evaluations on flexibility and performance. The packet processing engine's architecture will also be considered during the remainder of this reporting year. The goal is to have both SDR and packet processor FPGA implementations tested and evaluated by the end of 2005.

Adaptive Network Protocols

In parallel to SDR and packet processor design work described above, a project has been started on adaptive network protocols and related algorithms [10]. In particular, we are studying the concept of an adaptive wireless network bootstrapped from the CSCC etiquette protocol previously developed at WINLAB. The CSCC protocol (which uses a broadcast beacon mechanism to inform neighboring radios of signal properties) is being extended to include information necessary for self-organization into a collaborative network of cognitive radios. Information on transmit power, PHY speeds, channel quality and aggregated routing information is added to the beacon to facilitate self-organization.

A preliminary evaluation of the protocol concepts is planned for year 2 of the project using a GNU radio extension to the ORBIT radio grid testbed. A GNU radio kit has been procured and an RF front end module is being developed for subsequent use as software defined ORBIT radio node extension.

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consumption. As a result, a "heterogeneous block-based architecture", which would help implement SDR baseband processing in an efficient way, is proposed.

An alternative approach of SDR system design was proposed in [2-9].

3 Heterogeneous block-based architecture

The heterogeneous-block based architecture (see Figure 1.2 below) combines a general microprocessor with special purpose hardware blocks. The microprocessor containing multiplier/accumulator units handles control intensive operations such as channel estimation, synchronization, and programming and interconnection of the heterogeneous blocks, while data intensive operations are handled by the heterogeneous blocks. The following heterogeneous-blocks have been identified:

1. **Channelization Block**: A configurable multi-stage filter used to select a sub-band and/or decimate the input signal for different standards.
2. **FFT/MWT Block**: A configurable architecture which can handle FFT operations used in OFDM and also handle the modifier Walsh transform used in 802.11b.
3. **Rake Block**: A generic four finger Rake accelerator for channel estimation, de-spreading in DSSS and CDMA.
4. **Interleaver Block**: Using a block-based memory and multiplexer-based address handler, a multi-mode architecture can handle de-interleaving for different standards.
5. **Data and Channel Encoding /Decoding Block**: A configurable architecture can handle both Viterbi (for 802.11a) and Encoder/Turbo Decoder (for WCDMA). Both the Data and Channel Encoder have a similar connection pattern, but only the Data Encoder needs feedback. A common block is proposed which can be configured in one clock cycle to perform either of the two functionalities.
6. **Detection and Estimation Block**: Common interference detection block.
7. A simple crossbar-based reconfigurable interconnect is proposed to connect different blocks and the processor.

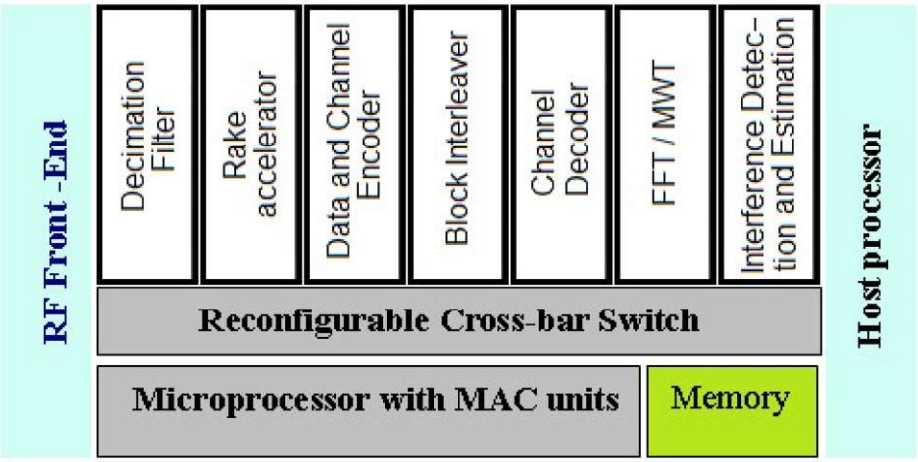

Fig. 2. Heterogeneous Blocks based Baseband Processor Architecture

combination of FPGA for hardware implementation and embedded RISC for software implementation. Embedded RISC cannot match the cost and power efficiency of a DSP, but it was felt that ease of programming was of more importance in an experimental platform – especially one that would be used by students. The group also decided to aim for tri-band (700 MHz, 2.4 GHz and 5.1 GHz) capabilities using a novel MEMS device – this was viewed as an important flexibility feature for an experimental platform of this type. The analog front-end would also support two channels, one for measurement and one for data, with bandwidths selectable in 1 MHz increments.

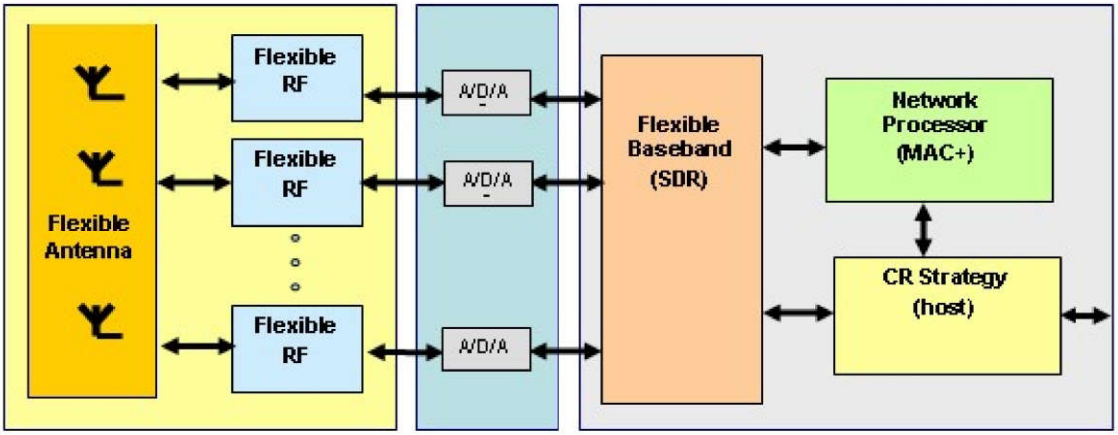

Fig. 1. Architecture of network-centric cognitive radio platform

2 Hardware architecture

Even though the prototyping effort is focused on an FPGA-based design, the architectural benefits of custom integrated circuitry, primarily related to power consumption and the silicon area, which are important performance parameters for hardware designs used in mobile/portable platforms are also explored. The approach that have been chosen to take involves identifying the hardware architecture appropriate for low-power configurable design based on heterogeneous blocks (i.e. blocks that are highly optimized for a particular function, yet flexible enough to support a variety of configuration parameters) as a compromise for the tradeoff between programmability and power consumption/area. In addition to fast prototyping, the additional benefits of using modern FPGAs (e.g. Xilinx Virtex 4) are the availability of highly optimized features implemented as non-standard configurable logic blocks (CLB) like phase-locked loops, low-voltage differential signal, clock data recovery, lots of internal routing resources, hardware multipliers for DSP functions, memory, programmable I/O, and microprocessor cores. These advantages simplify mapping from hierarchical blocks to FPGA resources.

The hardware design effort started with an evaluation of architectures presently available for baseband SDR processing at rates of 50-100 mbps. All these architectures use massive hardware parallelism to sustain high data rate. The baseband processing requirements of different wireless standards such as 802.11a/b, Bluetooth and WCDMA were analyzed carefully and it was concluded that different stages of baseband processing have very different hardware needs. Thus, using a generic hardware design leads to inefficient usage of chip area and power

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HIGH PERFORMANCE COGNITIVE RADIO PLATFORM

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The network-centric cognitive radio architecture under consideration in this article is aimed at providing a high-performance platform for experimentation with various adaptive wireless network protocols ranging from simple etiquettes to more complex ad-hoc collaboration [1]. Particular emphasis has been placed on high performance in a networked environment where each node may be required to carry out high throughput packet forwarding functions between multiple physical layers. Key design objectives for the cognitive radio platform include:

- multi-band operation, fast frequency scanning and agility;
- software-defined modem including waveforms such as DSSS/QPSK and OFDM operating at speeds up to 50 Mbps;
- packet processor capable of ad-hoc packet routing with aggregate throughput ~100 Mbps;
- spectrum policy processor that implements etiquette protocols and algorithms for dynamic spectrum sharing.

The cognitive radio prototype's architecture is based on four major elements [1]: (1) MEMS-based tri-band agile RF front-end, (2) FPGA-based software defined radio (SDR); (3) FPGA-based packet processing engine; and (4) embedded CPU core for control and management. These components will be integrated into a single prototype board, which leverages an SDR implementation.

1 Cognitive Radio Architecture & Design

The network-centric cognitive radio architecture under consideration in this article is aimed at providing a high-performance platform for experimentation with various adaptive wireless network protocols ranging from simple etiquettes to more complex ad-hoc collaboration. The basic design provides for fast RF scanning capability, an agile RF transceiver working over a range of frequency bands, a SDR modem capable of supporting a variety of waveforms including OFDM and DSSS/QPSK, a packet processing engine for protocol and routing functionality, and a general purpose processor for implementation of spectrum etiquette policies and algorithms. The proposed architecture is shown in Figure 1.

In the original proposal, the need for a baseband and network processor board is identified that would interface to the RF front-end and allow dynamically reconfigurable software and hardware implementations of multiple wireless links supporting individual data rates up to 50Mb/s and a maximum aggregate data rate of 100 Mb/s. It was expected that this board would contain some mix of DSP and FPGA blocks together with their required memories. At the first coordination meeting in 4Q2004, we made a decision to avoid the use of DSP's because of the difficulty associated with programming these devices. Rather, we decided to use a

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